REMARKS

Status of the Claims

Claims 1-30 are currently present in the Application, and claims 1, 11, and 21 are independent claims. No claims have been amended, canceled, or added in this Response.

Information Disclosure Statements

Applicants note that additional Information Disclosure Statements (IDSs) were filed on July 16, 2007, October 2, 2007, and December 27, 2007. Each IDS included a Form PTO-1449. However, the initialed copies of these forms have not been returned to Applicants. Applicants have checked the Image File Wrapper to confirm that each of these IDSs and its associated form PTO-1449 is included in the Image File Wrapper for the Application. Applicants respectfully request that the IDSs be considered, and the initialed Forms PTO-1449 be returned with the next action.

Claim Rejections – Alleged Obviousness Under 35 U.S.C. § 103

Claims 1-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mochizuki, U.S. Patent No. 5,490,278 (hereinafter Mochizuki) in view of Nakanishi, U.S. Patent No. 5,887,186 (hereinafter Nakanishi) and further in view of Matena et al., U.S. Patent No. 7,165,108 (hereinafter Matena). Applicants respectfully traverse the rejections under 35 U.S.C. § 103.

Applicants teach and claim that a virtual machine program is loaded into a second processor's local memory. Software code data is then processed by the second processor using the virtual machine program. This processing results in executable instructions that are then written to a memory location accessible by a first processor and executed by the first processor. None of the cited art teaches or suggests the claim elements found in Applicants' independent claims. Further, the Office Action does not cite any specific portions of Mochizuki, Nakanishi, or Matena as teaching or suggesting

Applicants' claim elements. Rather, the Office Action refers to the abstracts of these references (see Office Action, page 3).

The Office Action further states that:

> "Moch and Nak teach tightly coupled heterogeneous processors and processing requests between the two processors and the interactions and processing between the processors. But neither Moch and Nak teach a load balancing with virtual machine program. It Matena (sic) who teaches load balancing." (Office Action, page 3).

For the reasons discussed below, Applicants disagree that Mochizuki and Nakanishi teach heterogeneous processors. Regarding the citation to Matena and the discussion of "load balancing," Applicants respectfully note that there is no reference to "load balancing" in the claims.

Using independent claim 1 as an exemplary claim, Applicants teach and claim the following:

- loading, at a second processor, a virtual machine program into a local memory corresponding to the second processor;
- receiving, at the second processor, a code processing request requested by a first processor, wherein the first and second processors are heterogeneous processors within a computer system that share a common memory;
- reading, from the common memory shared by the first and second processors, software code data corresponding to the request, the software code data including virtual machine code adapted to be processed by the virtual machine program;

- writing the software code data corresponding to the request to the local memory corresponding to the second processor in response to the request;
- processing the software code data by the second processor, wherein the processing includes processing the virtual machine code at the second processor using the virtual machine program, the processing resulting in executable instructions;
- writing the executable instructions to a memory location accessible by the first processor; and
- executing, at the first processor, the executable instructions.

As an initial matter, none of the cited art appears to teach or suggest heterogeneous processors, as taught and claimed by Applicants. Mochizuki purports to teach using parallel processing to solve linear equations (see Mochizuki, Abstract). Although Mochizuki discusses the use of preprocessing sections, an updating section, and a back-substitution section (Mochizuki, col. 2, line 32 through col. 3, line 24), there is no indication that these sections include heterogeneous processors. The Office Action cites Mochizuki at Figure 1, reference numeral 1, as teaching heterogeneous processors (Office Action, page 3), however, reference numeral 1 points to a memory and not to a processor. Nakanishi purports to teach the use of a memory-distributed parallel processor to solve linear equations (see Nakanishi, Abstract). However, the processors in Nakanishi do not appear to be heterogeneous processors (Nakanishi, col. 2, lines 1-10). Matena purports to teach load balancing in a JAVA environment using various service modules (Matena, col. 2, lines 35-67 and col. 3, lines 1-38). Matena discusses service modules running on different servers, but Matena does not disclose, or even mention, "heterogeneous processors," as taught and claimed by Applicants. Because none of the cited references disclose the use of heterogeneous processors,

Applicants respectfully submit that none of the references teaches or suggests "receiving, at the second processor, a code processing request requested by a first processor, ***wherein the first and second processors are heterogeneous processors*** within a computer system that share a common memory," as taught and claimed by Applicants in independent claims 1, 11, and 21.

Applicants further submit that none of the cited art teaches or suggests "loading, at a second processor, ***a virtual machine program*** into a local memory corresponding to the second processor," and then "processing the software code data by the second processor, wherein the processing includes ***processing the virtual machine code at the second processor using the virtual machine program***, the processing resulting in executable instructions," as taught and claimed by Applicants. A close reading of both Mochizuki and Nakanishi shows no mention of a virtual machine. As known to those skilled in the art, a virtual machine engine is designed and written for a particular processor, hardware platform, and/or operating system (see Applicants' specification on page 2, line 27 through page 3, line 10 and also on page 48, lines 4-15). An application program written for a particular virtual machine, such as a Java Virtual Machine (JVM), can be run on various platforms, so long as it is run using an interpreter or is compiled for the particular platform before being run. Matena briefly mentions a Java Virtual Machine (JVM) at col. 7, lines 39-45, however, Matena does not go into any detail regarding the operating of this JVM.

As noted above, Applicants teach and claim that a virtual machine program is loaded into the second processor's local memory. The software code data is then processed by the second processor using the virtual machine program. This processing results in executable instructions that are then written to a memory location accessible by the first processor and executed by the first processor. None of the cited references, either alone or in combination, teaches or suggests any of these elements of Applicants' independent claims. The Office Action does not cite any specific portions of Mochizuki, Nakanishi, or Matena as teaching or suggesting these claim elements. Therefore, Applicants respectfully submit that the cited art does not teach or suggest "loading, at a

second processor, ***a virtual machine program*** into a local memory corresponding to the second processor," and then "processing the software code data by the second processor, wherein the processing includes processing the virtual machine code at the second processor ***using the virtual machine program***, the processing resulting in executable instructions," as taught and claimed by Applicants.

For the reasons set forth above, Applicants respectfully submit that independent claims 1, 11, and 21, and the claims which depend from them, are patentable over Mochizuki in view of Nakanishi and Matena, and respectfully request that they be allowed.

Notwithstanding the patentability of claims 4-6, 14-16, and 24-26 based on the above discussion, Applicants would like to further address these claims. Claims 4, 14, and 24 add elements including:

- running a first program;
- in response to running the first program, identifying a call to a software effect corresponding to the software code data; and
- loading the software code data into the common memory, wherein the processing of the software code data occurs during the running of the first program and wherein the processing is completed prior to the first program calling the software effect.

Claims 5, 6, 15, 16, 25, and 26 add further elements having to do with multimedia effects. Neither Mochizuki nor Nakanishi includes any discussion regarding calling software effects, such as multimedia effects. As noted above, Mochizuki and Nakanishi disclose methods for solving linear equations, and do not appear to have anything to do with software effects, and in particular with multimedia effects. Nor does the additional citation of Matena overcome the deficiencies of Mochizuki and Nakanishi. The Office Action cites Matena as disclosing "what to balance" (see Office Action, page 4). The

Office Action also refers to Figure 23, which is not a figure that is present in Matena. Applicants respectfully note that Matena does not teach or suggest the elements of claims 4, 14, and 24. Applicants further note that no citations are made to any of the cited references to reject claims 5, 6, 15, 16, 25, and 26. Applicants respectfully request that the Examiner clarify exactly what portions of the cited references are being used to reject claims 4-6, 14-16, and 24-26.

Based on the above discussion, Applicants respectfully submit that claims 4-6, 14-16, and 24-26 are patentable over Mochizuki in view of Nakanishi and Matena.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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